Andrew Stites

EEE 64 – CpE64 Section 2

Wednesday

Lab 10-11

Samuel Wekanda

Lab Objective/Goal:

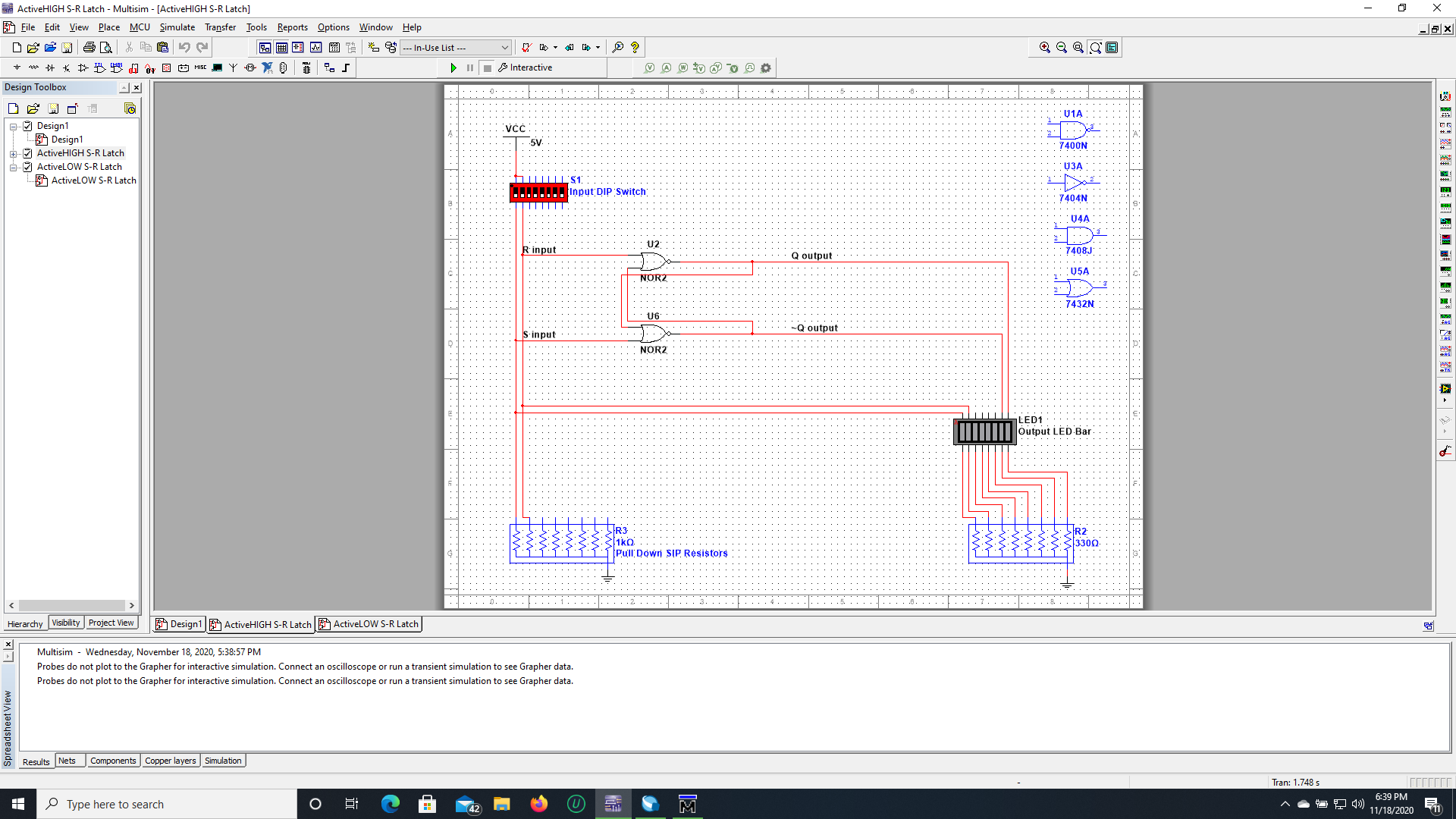
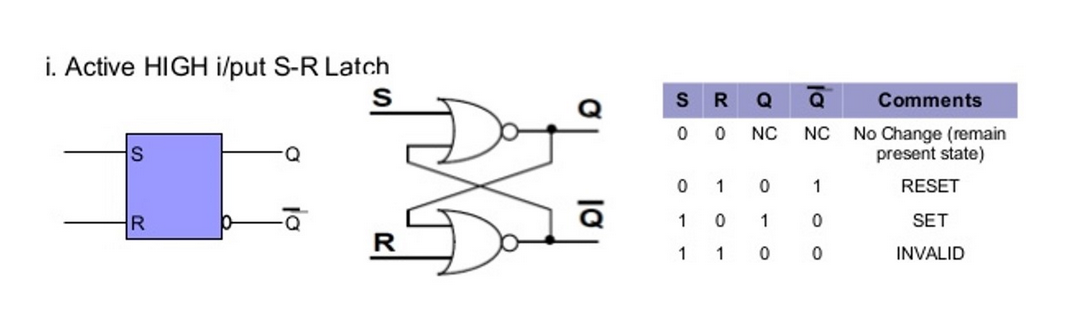
Design an active High SR Latch and an active Low SR Latch combinational circuit using Multisim and utilize Modelsim to display the waveform.

Lab Preparations and Challenges:

I created two different Multisim files. One being the active High SR Latch that consisted of two NOR gates with the outputs of each going to the other NOR gate. The other file consisted of two NAND gates with the outputs of each going to the other NAND gate. In Quartus, I created two Verilog HDL files named “HighLatch” and “LowLatch”, then coded my combinational logic designs which both compiled successfully. I created two more Verilog HDL files named “HighLatch\_tb()” and “LowLatch\_tb()” which were used as the testbenches for the initial Verilog HDL files. Once they compiled successfully, I ran simulations through Quartus that opened up ModelSim. I compiled the Verilog HDL files individually named “HighLatch\_tb()” and “LowLatch\_tb()”, then accessed them under the “work” drop down section in the Library module. I copied the variables to the Wave editor so that they could be shown utilizing green lines that are either HIGH for 1 or LOW for 0. I ran the simulation at “100 ps” to fully simulate all inputs.

Lab Results:

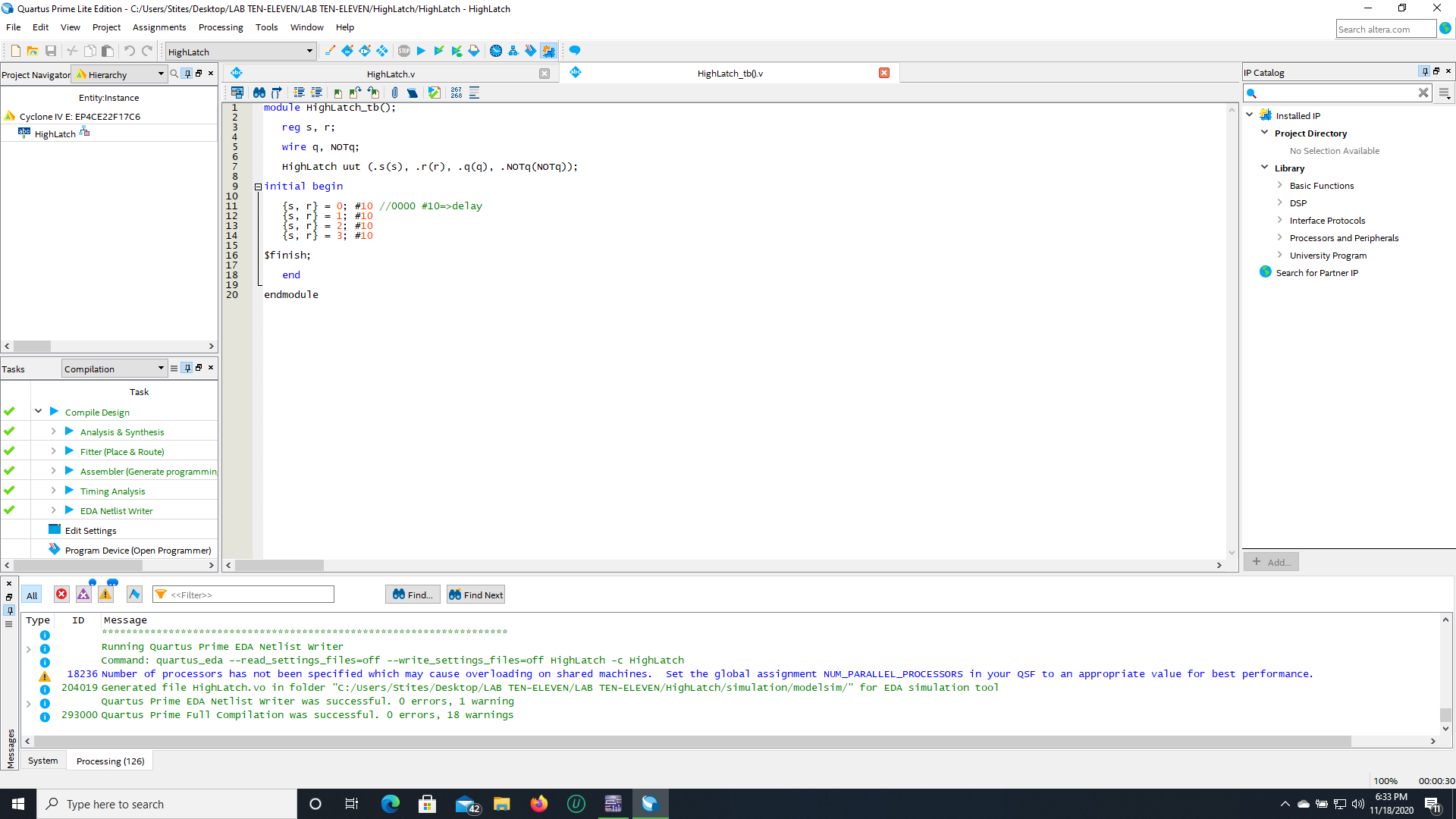
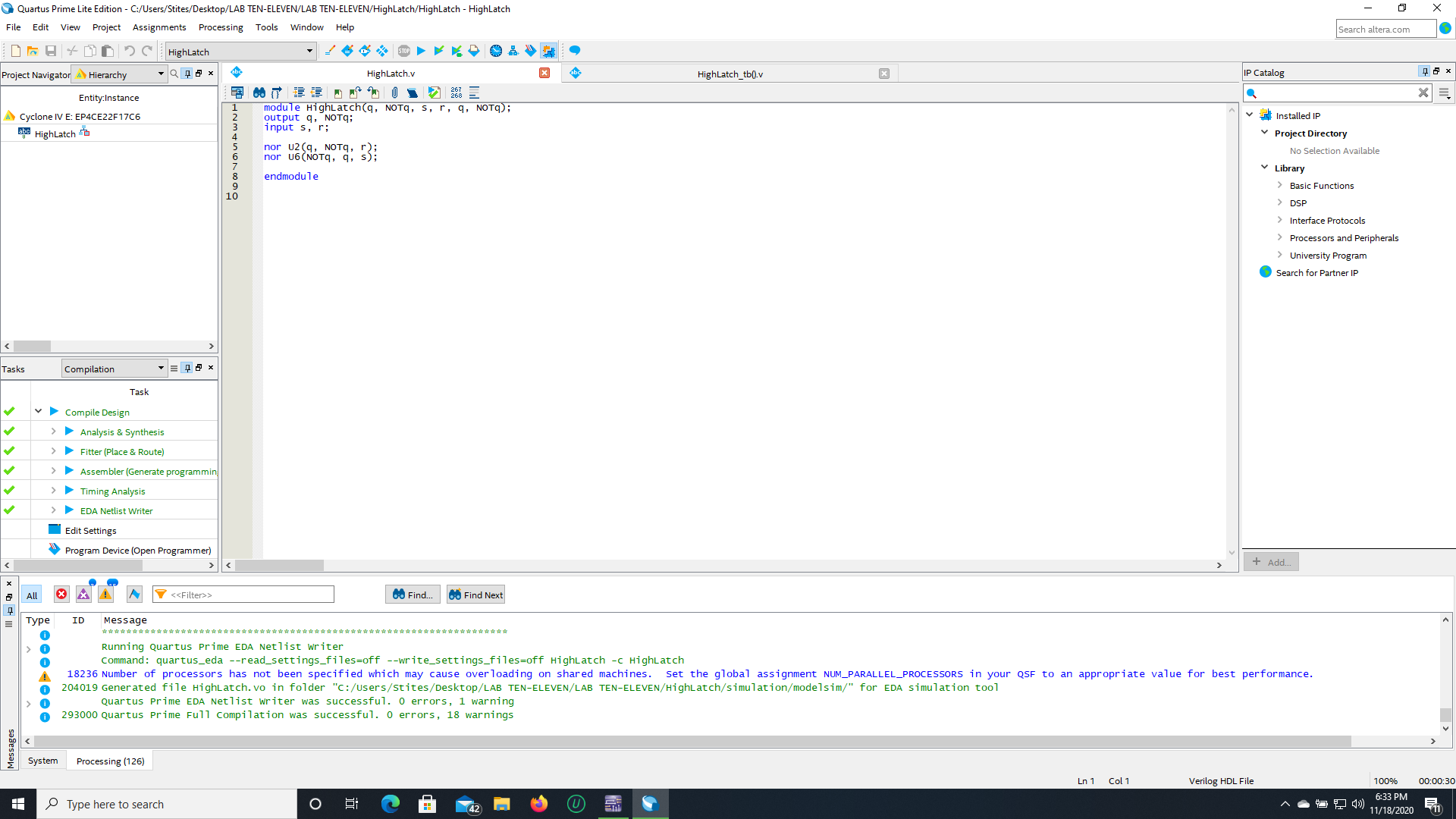
**Active High SR Latch:**



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S | R | Q | NotQ | Comments |
| 0 | 0 | No Change | No Change | Latched State |
| 0 | 1 | 0 | 1 | Reset |
| 1 | 0 | 1 | 0 | Set |
| 1 | 1 | 0 | 0 | Invalid |

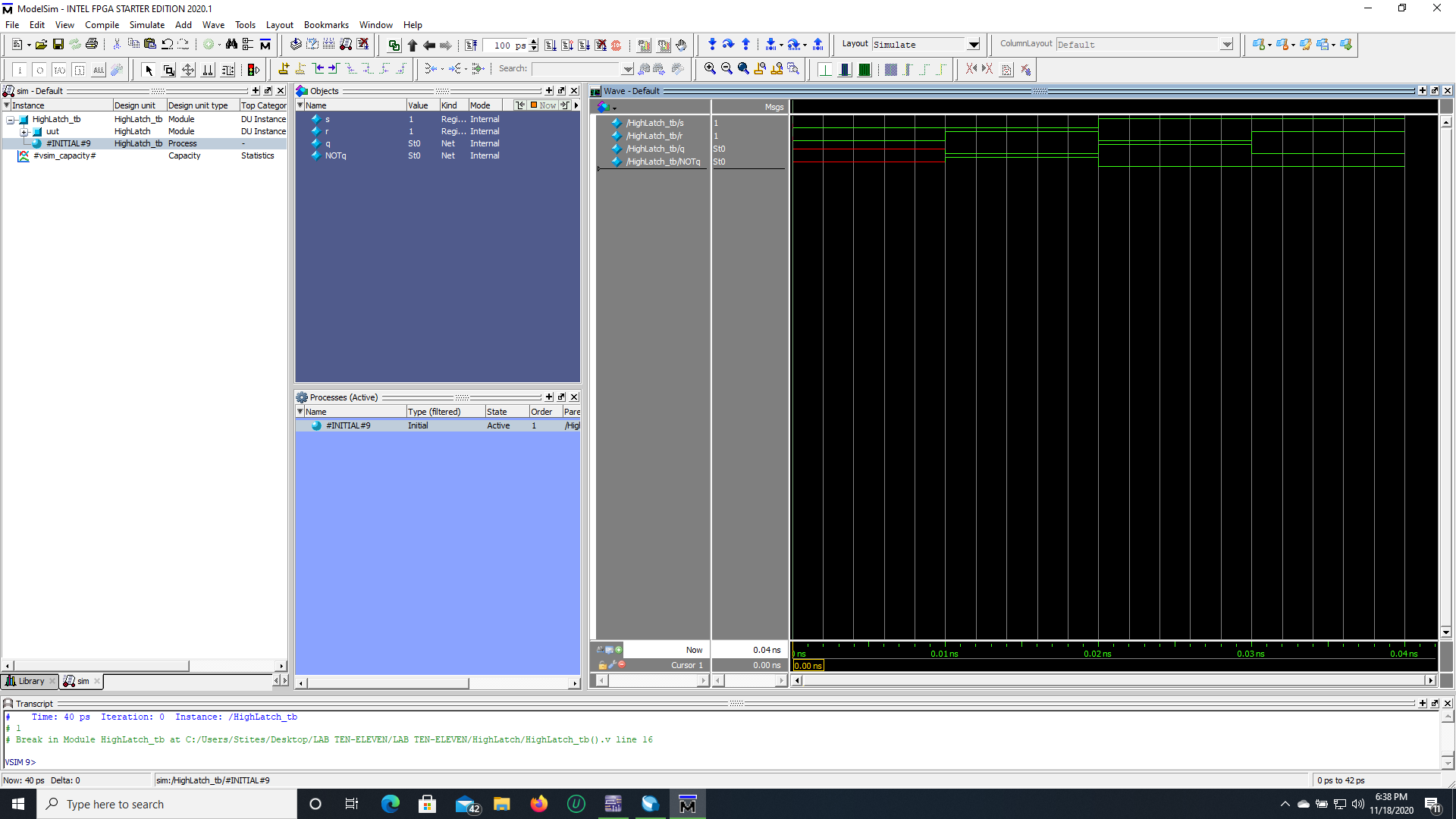
The Multisim file shown above shows the combinational circuit of the active High SR Latch. The table below it shows the outputs showing the inputs of “S” and “R” from 00 to 11. The outputs were “Q” and “NotQ” which have a specific state depending on the input given.

**Modelsim HDL Verilog:**



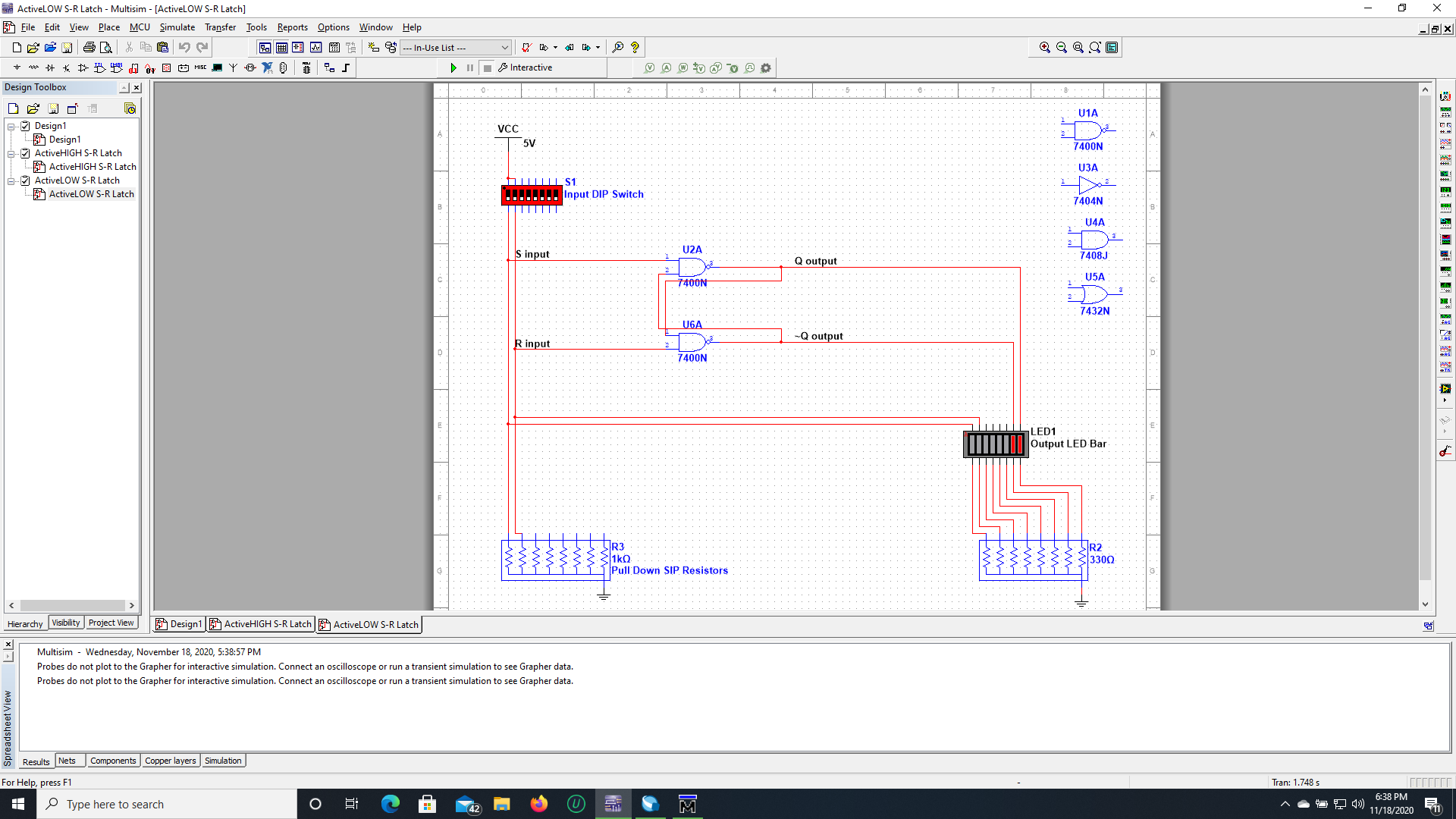
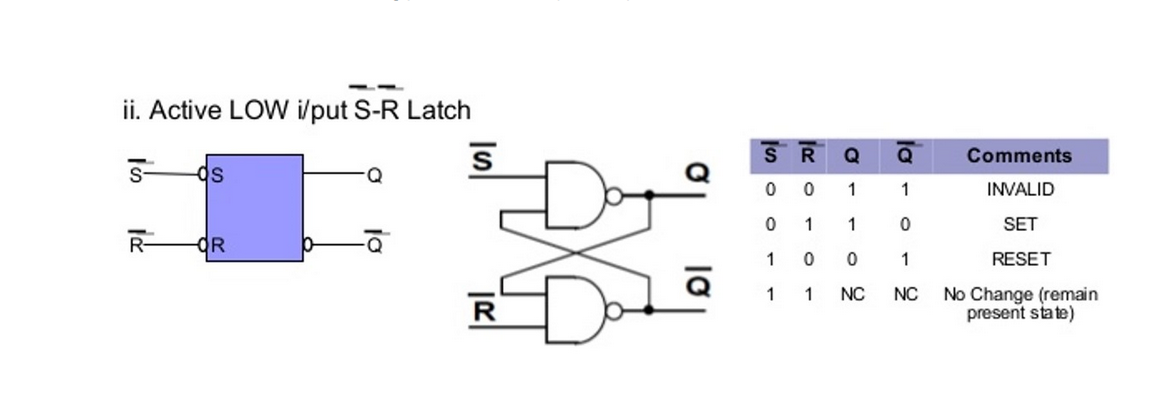
This portrays the combinational circuit that was created in Multisim written in Verilog HDL. The module is named “HighLatch” with outputs “Q” and “NotQ” and inputs “s” and “r”. Following suit are the NOR gates set-up with the output of “Q” going into the input of one NOR gate and the output of “NotQ” going into the other. This leads to the end of the module.

**Waveform Editor:**



The components of the combinational circuit have been implemented into the wave editor with the inputs “s” and “r” and the outputs “Q” and “NotQ”. This is using the compiled file “HighLatch\_tb()” for the simulation. The testbench allowed for the cycling from 00 to 11 in our initial Verilog HDL file that contained our combinational code setup. The wave form is presented portraying the inputs and output with all the lines being green except for the initial double Low input being red. This is due to the absence of a previous state in the SR Latch.

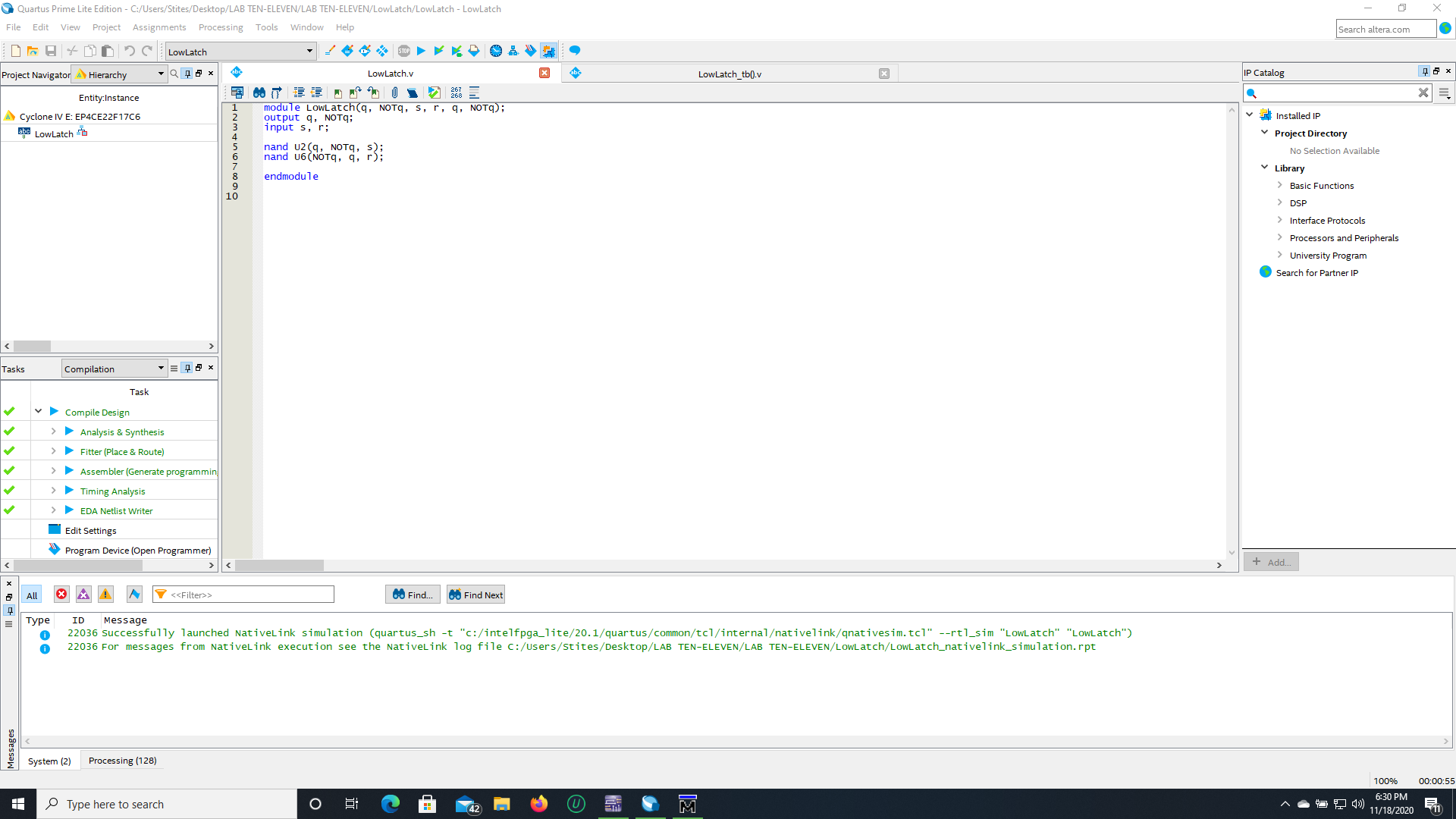
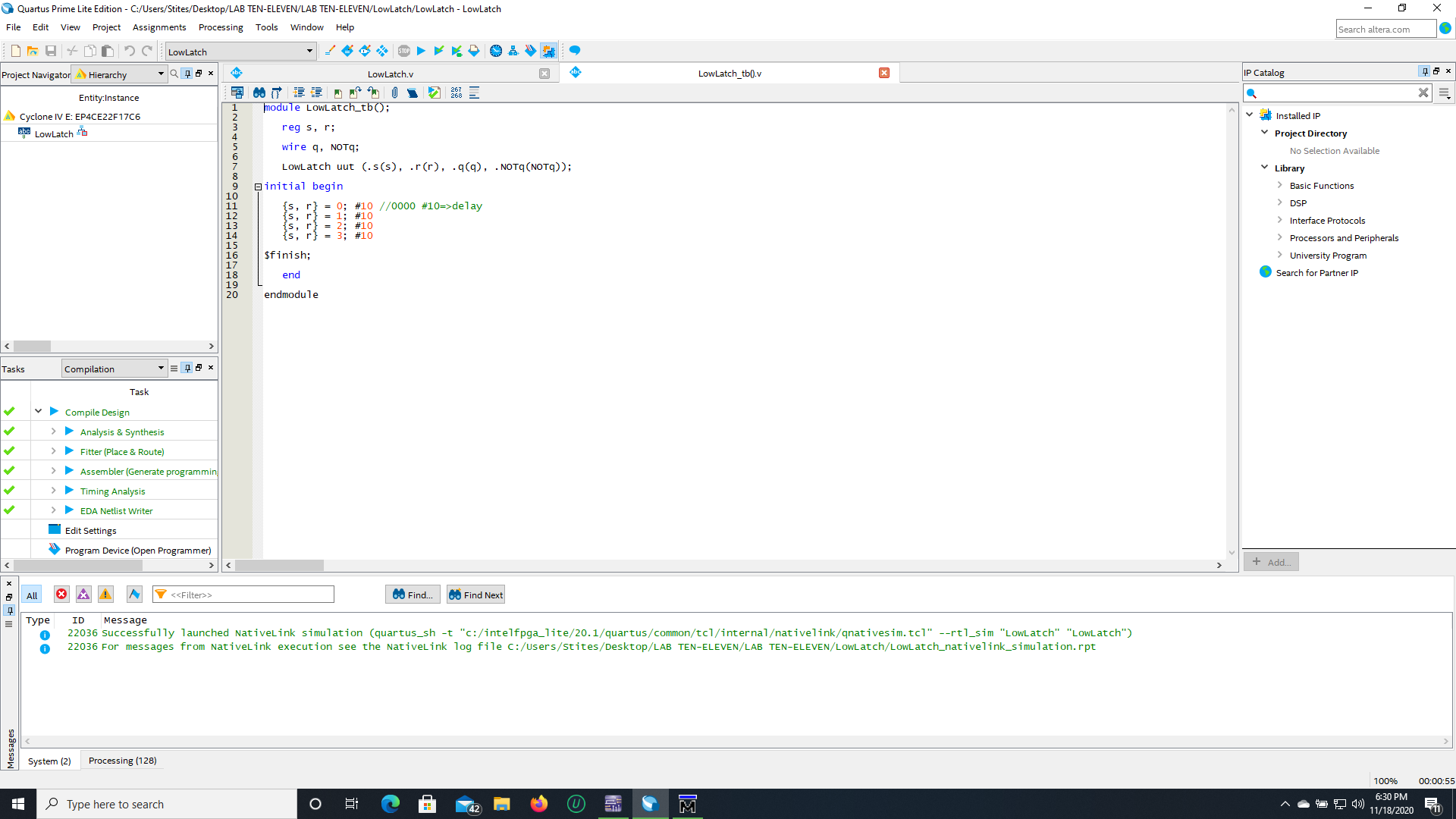
**Active Low SR Latch:**



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S | R | Q | NotQ | Comments |
| 0 | 0 | 1 | 1 | Invalid |
| 0 | 1 | 1 | 0 | Reset |
| 1 | 0 | 0 | 1 | Set |
| 1 | 1 | No Change | No Change | Latched State |

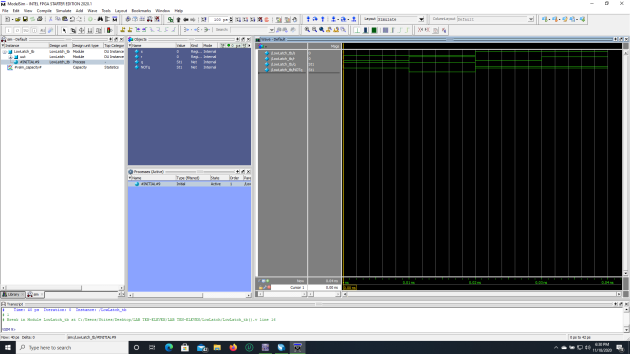
The multisim file shown above shows the combinational circuit of the active Low SR Latch. The table below it shows the outputs showing the inputs of “S” and “R” from 00 to 11. The outputs were “Q” and “NotQ”, which have a specific state depending on the input given.

**Modelsim HDL Verilog:**



This portrays the combinational circuit that was created in Multisim written in Verilog HDL. The module is named “LowLatch” with outputs “Q” and “NotQ” and inputs “s” and “r”. Following suit are the NOR gates set-up with the output of “Q” going into the input of one NOR gate and the output of “NotQ” going into the other. This leads to the end of the module.

**Waveform Editor:**



The components of the combinational circuit have been implemented into the wave editor with the inputs “s” and “r” and the outputs “Q” and “NotQ”. This is using the compiled file “LowLatch\_tb()” for the simulation. The testbench allowed for the cycling from 00 to 11 in our initial Verilog HDL file that contained our combinational code setup. The wave form is presented portraying the inputs and output with all the lines being green with the last part with the inputs being “11” being the latch state coping the last state. This is due to the presence of a previous state in the SR Latch.

Conclusion:

These labs were very straight forward due to the previous labs setting myself up with the knowledge and expertise to complete them. I learned a great amount of Quartus and ModelSim and feel confident regarding the future labs. Having an extra week to complete both labs made for a very relaxed work environment. I can conclude with having little trouble finishing both labs.